UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,485	01/12/2001	Nirav Dagli	ENTRDA.0012P	6559

7590 09/08/2004

Chad W. Miller
Weide & Associates, Ltd.
Phoenix Bldg., 11th Floor, Suite 1130
330 South 3rd Street
Las Vegas, NV 89101

EXAMINER	
WONG, BLANCHE	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,485	DAGLI ET AL.	
	Examiner	Art Unit	
	Blanche Wong	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *January 12, 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-21,23 and 25-35* is/are rejected.

7)☒ Claim(s) *12,13,22,24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#4/June 21'01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method and System for Tracking Data Using Shared Memory.

Claim Objections

2. Claim 1 is objected to because of the following informalities: misspelling. In claim 1, ln. 1, – queueing -- should be spelled "queuing." Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-5, 7-11, 14-18, 20,21,23,25-29** are rejected under 35 U.S.C. 102(b) as being anticipated by Yin (U.S. Pat No. 6,219,728).

With regard to claim 1, Yin discloses a method of packet (col. 3, ln. 48-50 and col. 4, ln. 39-40) queuing (queues 104, Fig. 2) in a packet processing device (switch 100, Fig. 2) comprising:

receiving (input ports IN1-M, col. 3, ln. 41; see also Fig. 2) a packet;

analyzing (the data cell are stored in a particular memory buffer, therefore it is inherent that there is some association between the data cell and the particular memory buffer, col. 4, ln. 20-26) the packet to determine a designated queue (particular memory buffer, col. 4, ln. 21) for the packet;

generating a packet identifier (the entries in the address queue, col. 4, ln. 20-21) based on the analyzing;

associating an address (the entries in the address queue point to a particular memory buffer within shared memory, col. 4, ln. 20-21, therefore, it is inherent that the entries is some sort of addressing; see also col. 4, ln. 44-49 and col. 5, ln. 8-10) to a shared memory with the packet identifier;

storing (col. 4, ln. 25-30) the packet identifier in the shared memory at the associated address; and

storing (col. 4, ln. 25-30) the associated address in the designated queue.

With regard to claims 2,23,28, Yin further discloses a FIFO device. Col. 3, ln. 67-col. 4, ln. 1.

With regard to claim 3, Yin further discloses type of service information. Col. 4, ln. 3-9; see also col. 6, ln. 5-6.

With regard to claim 4, Yin further discloses a controller 122 (input processor, Fig. 8A) and a FIFO device (col. 3, ln. 67-col. 4, ln. 1).

With regard to claim 5, Yin further discloses evaluating if an address is available ("provided that the appropriate address queue is not full" inherently means that an entry/address to an address queue might not be made available, col. 4, ln. 29-30; see also col. 7, ln. 46-47).

With regard to claim 7, Yin discloses a method for tracking data items (col. 3, ln. 48-50 and col. 4, ln. 39-40):

assigning (the data cell are stored in a particular memory buffer, therefore it is inherent that there is some association between the data cell and the particular memory buffer, col. 4, ln. 20-26) data items one or more designations (particular memory buffer, col. 4, ln. 21) of a plurality of designations;

for each designation, obtaining and assigning a memory address (the entries in the address queue point to a particular memory buffer within shared memory, col. 4, ln. 20-21, therefore, it is inherent that the entries is some sort of addressing; see also col. 4, ln. 44-49 and col. 5, ln. 8-10), the address corresponding to a location in a shared memory;

tracking (addresses are kept as entries in address queues) each assignment of designation of data items;

storing (col. 4, ln. 25-30) a record of each designation and assigned memory address in the shared memory at the obtained memory address, wherein the shared memory stores a plurality of assignments of designations (output ports OUT1-N, col. 3, ln. 44; see also Fig. 2).

With regard to claim 8, Yin further discloses a plurality of queues (address queues 104, Fig. 2).

With regard to claims 9 and 21, Yin further discloses an order of receipt (FIFO is an order of receipt, col. 3, ln. 67-col. 4, ln. 1).

With regard to claim 10, Yin further discloses a plurality of locations (plurality of output ports, col. 3, ln. 44).

With regard to claim 11, Yin further discloses deleting one or more records from the shared memory if the shared memory is full. Col. 4, ln. 66-col. 6, ln. 14; see also Fig. 5A-7B.

With regard to claims 14 and 15, Yin discloses a shared memory 102 (also shared memory in Fig. 2) and a plurality of queues (address queues 104, Fig. 2) configured for use in a data item processing device (switch 100, Fig. 2) comprising:

a shared memory 102 configured to stored at least one data item identifier (addressing), the memory having memory locations defined by memory addresses (the entries in the address queue point to a particular memory buffer within shared memory, col. 4, ln. 20-21, therefore, it is inherent that the entries is some sort of addressing; see also col. 4, ln. 44-49 and col. 5, ln. 8-10);

a plurality of queues (address queues 104, Fig. 2), at least one queue configured to track the order of receipt (FIFO is an order of receipt, col. 3, ln. 67-col. 4, ln. 1) of at least one data item identifier assigned thereto by storing memory addresses; and

control logic 122 (input processor, Fig. 8A) configured to initiate storage of at least one data item identifier in shared memory based on an evaluation of the data item identifier or the data item identified by the data item identifier and assign memory address at which data items are stored to one or more queues;

as recited in claim 14.

With regard to claims 16,18,26, Yin further discloses a FIFO memory structure. Col. 3, ln. 67-col. 4, ln. 1.

With regard to claim 17, Yin further discloses a memory address allocation unit 128, Fig. 8A.

With regard to claim 20, Yin discloses a queue (address queues 104, Fig. 2) system configured to utilize a shared memory 102 comprising:

a shared memory 102, Fig. 8A wherein items stored in shared memory are identified by a memory address;

two or more FIFO queues (queues 104 in Fig. 2; FIFO, col. 3, ln. 67-col. 4, ln. 1);

an address allocation unit 128 (shared memory usage monitor, Fig. 8A; see also col. 6, ln. 36-40) configured to allocate memory addresses;

a controller 122 (input processor, Fig. 8A; see also col. 6, ln. 15-39) configured to:

receive (cell arrival, Fig. 8A) and analyze (col. 6, ln. 17-20) packet data corresponding to a packet;

request an address (col. 6, ln. 19-20) from the allocation unit 128 (shared memory usage monitor, Fig. 8A; see also col. 6, ln. 32-35)

associate (add the address to the appropriate address queue, col. 6, ln. 20-21) the address with a packet identifier;

assign (add the address to the appropriate address queue, col. 6, ln. 20-21) the address to one or more of the queues based on the analysis of the packet data; and

initiate storage (add the address to the appropriate address queue, col. 6, ln. 20-21) of the packet identifier in shared memory at the address associated with the packet identifier.

With regard to claim 25, Yin discloses a FIFO (Col. 3, ln. 67-col. 4, ln. 1) queue (queues 104, Fig. 2) system having a shared memory 102 (also shared memory in Fig. 8A) comprising:

a controller 122 (input processor, Fig. 8A; see also col. 6, ln. 15-39) configured to received a packet, assigned the packet to a transmit priority queue, and store the packet in a first memory at a packet address;

at least one transmit priority queue (QoS, col. 4, ln. 3-9; see also col. 6, ln. 5-6) having order tracking system and an allocation unit interface, wherein the at least one transmit priority queue is configured to store the packet address in a shared memory;

a shared memory 102 (also shared memory in Fig. 8A) configured to store received packet addresses at memory locations in the shared memory; and

an allocation unit 128 (shared memory usage monitor, Fig. 8A; see also col. 6, ln. 32-35) configured to interface with the at least one transmit priority queue to allocate memory addresses for the shared memory to the at least one transmit priority queue.

With regard to claim 27, Yin further discloses RAM. Col. 3, ln. 55.

With regard to claim 28, Yin further discloses a transmit (cell departure, Fig. 8A) module.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 6,19,30-35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yin in view of Hoglund et al. (U.S. Pat No. 6,747,984).

With regard to claim 30, Yin discloses a method of transmitting information identified by a next-out (FIFO queuing) item from a queue, the queue utilizing a shared memory comprising:

requesting a next-out (FIFO queuing) item from the designated queue (particular memory buffer, col. 4, ln. 21), the next-out item identifying a memory address to a shared memory (col. 4, ln. 30-32);

retrieving (col. 5, ln. 8-10) the data item stored in the shared memory at the memory address identified by the next-out item from the queue; and

transmitting (col. 5, ln. 8-10) information stored at a location identified by the data item.

However, Yin fails to expressly show designating a queue with transmit priority.

Hoglund discloses designating a queue with transmit priority (priority scheme, col. 5, ln. 58 and col. 7, ln. 56-61).

A person of ordinary skill in the art would have been motivated to employ Hoglund in Yin in order to obtain a priority scheme for transmission. The suggestion/motivation to do so would have been to provide for transferring data between nodes where overhead is eliminated. Hoglund, col. 2, ln. 24-26. At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Yin and Hoglund to obtain the invention as specified in claim 30.

With regard to claim 31, Yin further discloses an address (the entries in the address queue point to a particular memory buffer within shared memory, col. 4, ln. 20-21) to shared memory 102 (also shared memory in Fig. 8A).

With regard to claim 32, Yin further discloses a packet (col. 3, ln. 48-50 and col. 4, ln. 39-40).

With regard to claim 33, Yin further discloses the queues stores queue items that identify information that shares a similar attribute. (QoS differentiating the queues, Col. 4, ln. 3-9; see also col. 6, ln. 5-6)

With regard to claim 34, Yin further discloses an address (the entries in the address queue point to a particular memory buffer within shared memory, col. 4, ln. 20-

21) to shared memory, data item comprise address to where information is stored in a second memory, and the shared memory stores data items.

With regard to claim 35, Hoglund further discloses the plurality of queues sharing the shared memory to store data items to thereby reduce the total amount of memory required. Fig. 3-5.

With regard to claim 6, Hoglund discloses information regarding the packet length (frames have delimiters, col. 4, ln. 54).

With regard to claim 19, Hoglund discloses a transmit logic (transmit controller 300, Fig. 3).

Allowable Subject Matter

7. **Claims 12,13,22,24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Johnson et al. (U.S. Pat No. 6,570, 853) discloses a method and apparatus for transmitting data to a node in a distributed data processing system.

Sakurai et al. (Pub No. 2001/0005386 A1) discloses an ATM cell-switching system comprising: a shared buffer memory, a queue chain, a memory control circuit, and an identifier.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blanche Wong whose telephone number is 571-272-3177. The examiner can normally be reached on Monday through Friday, 830am to 530pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BW
September 2, 2004

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600